VERDI-3: new improvements in multi-detector readout ASIC

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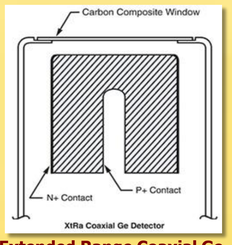
SUMMARY: In this work we present the circuit VERDI-3 (Versatile Readout for Detector Integration -3), an integrated circuit developed to provide a unique readout solution for different families of radiation detectors, from nitrogen-cooled Ge and Si(Li) detectors, to silicon drift detectors (SDDs), to scintillation detectors, to photomultipliers tubes and others. The detectors can have an output capacitance from 0.1pF to 39pF, while the energy range spreads from 300eV to 3MeV with both signal polarities, positive and negative. The readout scheme can be pulsed-reset or continuous-reset with an optional external zero-network. The circuit includes 8 channels, each one composed by a hybrid charge preamplifier, a shaping amplifier, a baseline holder, a peak stretcher, an output power buffer and an RC integrator for external digital processing. The output of each channel may alternatively be multiplexed on a single output for low-speed, low-power random readout. Different settings, like gain, shaping time, preamplifier compensation, "gamma" or "x ray" readout mode and many others can be externally programmed by SPI for the specific detector to be readout. Only the input JFET, the feedback capacitor and the reset device are left external to the ASIC, to be chosen specifically for each detector.

Readout from Multiple Detector types

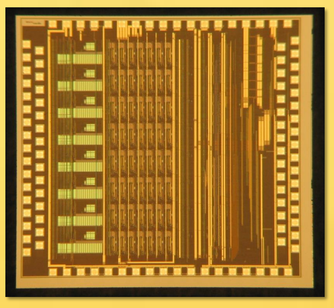
Silicon (Li) Detector System

SDDs



Extended Range Coaxial Ge Detectors (XtRa)

Cryo-Cooled Ge detectors (BEGe, REGe,LEGe, Ultra LEGe XtRa)



Microphotograph of Verdi ASIC
Dimensions: 3,47mm X 3,49mm

Verdi ASIC is a complete Analog Processing Circuit. Verdi allows the readout from 8 sensors in parallel with 8 independent outputs.

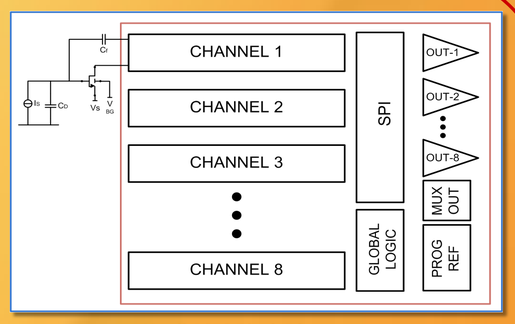
Verdi ASIC has been designed to process signal coming from 45 possible combination of detectors + Jfet pairs:

- **Fet g_m: from 2mS to 45mS**
- **C_{gs}: from 0.45pF to 25pF**
- **$C_{feedback}$: from 50fF to 1pF**
- **$C_{detector}$: from 200fF to 39pF**

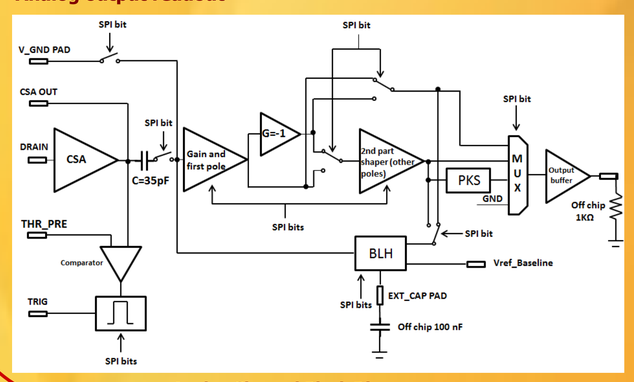
Asic programmable features – Analog Channel

Verdi ASIC:

- **8 complete analog channels for detectors signal processing**
- **2 modes of operation: Gamma Camera mode and Spectroscopy mode**
- **Embedded Logic to manage by ASIC itself both of operation modes**
- **128bits Serial register for ASIC function and setting programming**
- **Embedded ROM memory for stand-alone settings**
- **Selectable signal output: high performance Parallel Analog output or low power Serial Analog output**
- **Random access to each Analog output during Serial Analog output readout**



Verdi ASIC Block Diagram

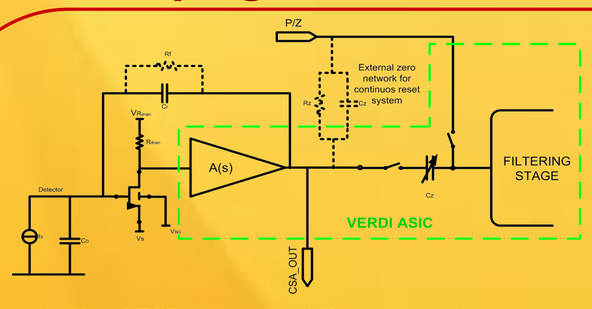


Analog Channel Block Diagram

Analog Channel:

- **Complete Architecture: from Preamplifier to Peak and hold circuit**
- **Process Positive or Negative signal (selectable)**
- **Selectable internal output for analog debug and mid-point processing pick-up node**
- **Selectable outputs: RC waveform, 7 poles Shaper and Peak Stretcher**
- **Programmable time window for processing chain inhibit during Pulsed reset operation**

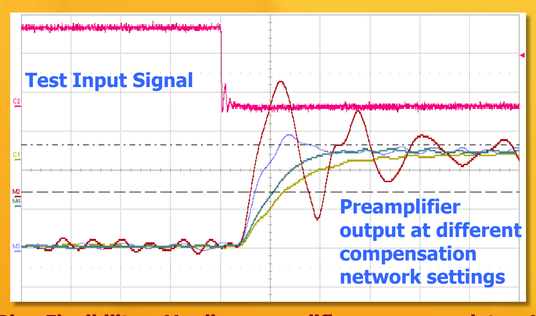
Asic programmable features – CSA stage



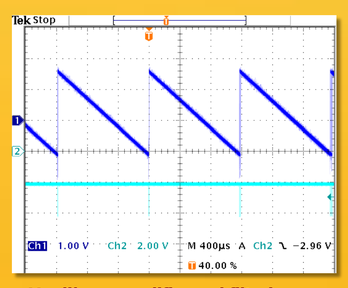
Verdi ASIC Front-end (green). Hybrid preamplifier (discrete Jfet) supports pulsed reset and continuous reset system.

The Charge Sensitive Amplifier has been designed on hybrid architecture (external JFET) and it allows pulsed reset system and continuous reset system. In order to accommodate the large variety of detectors+Jfet pairs the CSA can change the internal compensation network.

Moreover the CSA and the following filtering stage is able to process positive charge signals and negative charge signals

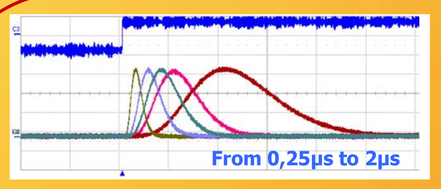


Big Flexibility: Verdi preamplifier accommodate 45 different combination of detector+Jfet pairs changing preamplifier feedback compensation by digital SPI

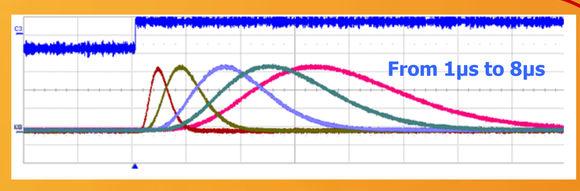


Verdi's preamplifier and filtering stage allow also negative ramps

Asic programmable features – Processing stage



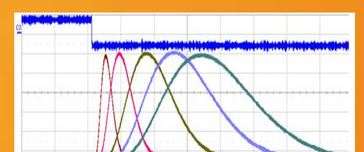
Internal shaper output waveform at 0.25µs, 0.5µs, 0.75 µs, 1µs and 2 µs shaping time.



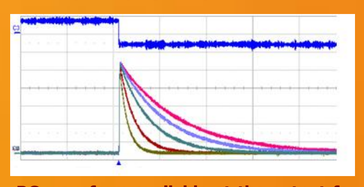
Internal shaper output waveform at 1µs, 2µs, 4µs, 6µs and 8 µs shaping time.

The processing filter stage is made up by Shaper and baseline holder circuit (BLH).

- **The programmable gain of the Shaper has <u>15 gain scale</u>: 20mV, 30mV, 50mV, 75mV, 95mV, 105mV, 125mV, 175mV, 195mV, 205mV, 225mV, 250mV, 270mV, 280mV and 300mV referred to the signal atr the output of the preamplifier (4bit in the SPI).**
- **The Shaper is a 7th order real poles semi-gaussian filter. It has <u>8 selectable shaping time</u>: 0.25µs, 0.5µs, 0.75µs, 1µs, 2µs, 4µs, 6µs, 8µs (3bit in the SPI).**
- **15*8=120 possible gain-shaping time combinations (both for the positive and negative input).**
- **The BLH stage holds the output of Shaper (or of the first integrator, programmable) around 0V compensating detector leakeage current within 100fA and 11nA (from -30°C to 45°C).**

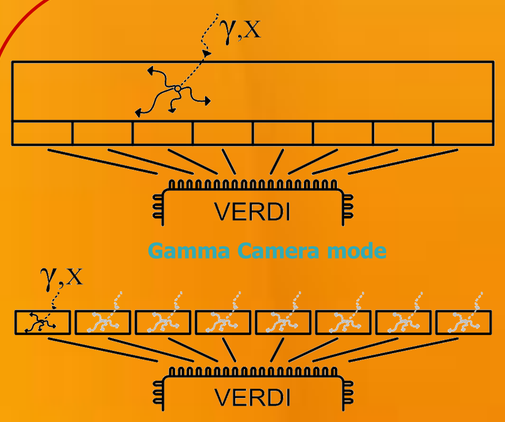


Internal shaper output waveform for a negative input (1µs, 2µs, 4µs, 6µs and 8 µs shaping time).



RC waveform available at the output for digital processing, available both for negative and positive inputs (in the figure above: 1µs, 2µs, 4µs, 6µs and 8 µs shaping time).

Mode of operation and SPI register with ROM memory



Gamma Camera mode operation:

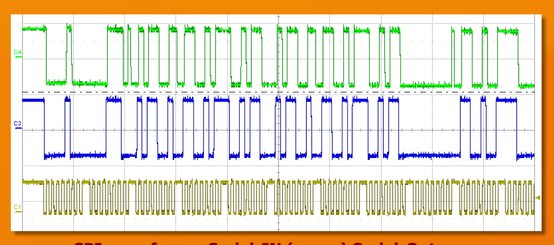
- **Collection of scintillator light from up to 8 sensors per ASIC**
- **Programmable Synchronous Signal to hold the 8 shaped pulse peak at given significant event**
- **High performance parallel readout or low power serial readout**

Spectroscopy mode operation:

- **8 independent signal processing channels per ASIC**
- **8 independent programmable event threshold to pick up only significant event**
- **High performance parallel readout or low power serial readout**

SPI register for ASIC programming:

- **128bits register for internal setting of Verdi ASIC**
- **Gain Setting – Shaping Time – Bias Currents setting – Threshold Voltages – Operation Mode**
- **Embedded 128bits ROM memory for stand-alone setting without SPI programming**



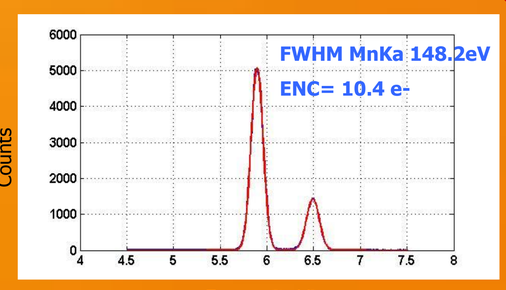
SPI waveforms: Serial-IN (green) Serial-Out (blue) and Serial-Clock (yellow) @ 500Kbits/s

Preliminary Spectroscopy results

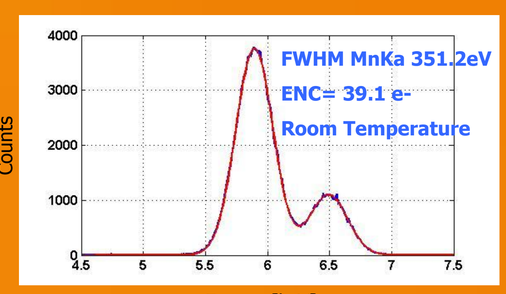
25mm² SDD, T_d=-30°C

Measurements with internal shaper: Fe55 Source with single anode SDD 25mm² at -30°C, comparison between the new version and an older one; the noise performance of the new one is comparable respect to external NIM acquisition system.

Tsh [µs]	0.25	0.5	0.75	1	2	4	6	8
FWHM [eV]	189.4	164.4	154.2	150.3	148.2	154.4	163.5	172.3



Energy spectrum with 55Fe source, shaping time 2µs.



Energy spectrum with 55Fe source at room temperature, shaping time 0.25µs.

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